Remarks/Arguments

The Office Action mailed March 28, 2007 has been reviewed and carefully considered.

Claims 1, 3, 8, 11, 13 and 14 have been amended. Claims 1-16 are now pending in this application. It should be noted that the applicants are not conceding in this application that the original claims are not patentable over the art cited by the examiner, as the present claim amendments have been made only to facilitate expeditious prosecution of the application. The applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

Reconsideration of the above-identified application, as herein amended and in view of the following remarks, is respectfully requested.

Prior to addressing the outstanding rejections, the applicants will briefly summarize the present principles to better assist the examiner in appreciating the differences between the claimed invention and the prior art references. The present principles include a method and system for increasing performance in a storage network by employing a cache system. A preferred embodiment of the present principles includes, inter alia, a storage mechanism (SAN, 12) and a local cache (14). The storage mechanism is the main storage for the system and the local cache mirrors at least some of the content stored on the storage mechanism. Users access the local cache in lieu of the storage mechanism whenever possible to reduce network traffic, thereby providing greater efficiency in the use of network resources.

Other components of a preferred embodiment include a SAN access manager (17), a cache manager (18), a write director (16), a read director (20), and a filler (24). The write

director writes input content to both the storage mechanism and the local cache. The read director receives requests for content from users and determines whether the requested content is in the local cache. If the content is in the local cache, then the local cache is accessed. If the content is not in the local cache, the read director directs the user to either the storage mechanism or the filler. The filler provides the user with filler content in the event that the storage mechanism is inaccessible due to bandwidth constraints. The cache manager maintains content coherency between the storage mechanism and the local cache to ensure that both storage mechanisms have up-to-date content. Additionally, when requested content is not found in the cache, the cache manager downloads the requested content to the cache and deletes least recently accessed content when necessary.

According to one aspect of the present principles, the SAN access manager monitors the read and write load to the storage mechanism and controls the read and write directors and the local cache manager in accordance with the storage mechanism read and write loading. One function of the SAN access manager is to reduce reading from, and writing to the SAN access mechanism during intervals of high bandwidth demand (see original claims 10 and 16). The SAN access manager determines intervals of high bandwidth by monitoring the number and type of read and write requests to the SAN access mechanism (see discussion below concerning the §112, first paragraph rejections of claims 10 and 16) (see also Specification, p. 3, line 16 and p. 4 lines 26-28).

Claim 14 stands objected because it appeared to be missing appropriate claim invention language because of a typographical error or an inadvertent exclusion of words or characters. Claim 14 has been amended in a way believed to overcome the rejection. Accordingly, the applicants respectfully request removal of the objection.

Claims 10 and 16 stand rejected under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement. Specifically, the examiner states that the disclosure fails to describe how the present principles determine "intervals of limited bandwidth" to reduce reading and writing. As stated above, the SAN access manager monitors the read and write load to the storage mechanism. (Specification, p. 3, line 16). In addition, the SAN access manager controls the reading from, and the writing of content to the SAN access mechanism during intervals of high bandwidth demand (Specification, p. 4, lines 26-28). One of ordinary skill in the art would recognize that monitoring the read and write load on the storage mechanism includes monitoring the number and type of read and write requests to the SAN access mechanism to determine levels of high bandwidth demand. Accordingly, claims 10 and 16 comply with the enablement requirement. Thus, withdrawal of the rejection of claims 10 and 16 on this basis is respectfully requested.

Claims 1, 2, 4-12, and 15-16 stand rejected under 35 U.S.C. §102(e) as being anticipated by Chiou, et al. (U.S. Patent No. 6,792,507) (hereinafter 'Chiou').

Chiou describes a caching system for accessing data across a network. The system according to Chiou includes a two-level caching system in which one cache is located near a requesting host and another cache is located near a main storage unit on a network. When the Chiou system receives a read request, it determines whether the requested data is located in the cache on the host. If the data is not on the host cache, then the request is forwarded to the storage cache. In the event that the host cache does not contain the requested data, the request is forwarded to the main storage unit.

Chiou also discloses a cache manager that manages the coherence between the data in the caches and the data in the main storage unit. Two ways coherence is accomplished in the system

includes updating or invalidating the data block or file in the cache (see Chiou, column 3, lines 24-28). The caches are updated or invalidated when a data block or file is written to the main storage device and the caches contain an older version of the data block or file (see Chiou, column 3, lines 24-28). The cache manager may update or invalidate the cache according to either a critical coherent mode or a non-critical coherent mode (Chiou, column 9, lines 24-29). In the critical coherent mode, the caches are updated prior to writing the data to the main storage device (Chiou, column 15, lines 3-5). Conversely, in the non-critical coherent mode, data is written to the main storage device before the caches are updated or invalidated (Chiou, column 15, lines 5-7).

The only way the system described in Chiou affects data writing to the main storage device is by changing the order in which the data is written to the main storage device and the caches. Chiou does not even remotely suggest reducing the number of writes on the main storage. Chiou merely discloses changing the order in which the content is downloaded within the system. Indeed, the system of Choiu services all write requests.

The SAN access manager, however, reduces the number of writes to the storage mechanism during intervals of high bandwidth demand. By monitoring and controlling the reading and writing to the storage mechanism, the SAN access manager may optimize bandwidth resources of the network. As discussed above, Chiou does not disclose or remotely suggest reducing the number of writes to the storage mechanism. Accordingly, the present principles are distinguished from Chiou at least because Chiou does not disclose reducing the writing to the main storage device.

Moreover, reducing the number writes on the main storage is not obvious in view of Chiou. Chiou's method of reducing network traffic congestion relies on the number and location

of caches with respect to the requesting host and the main storage unit. Based on Chiou, one of ordinary skill in the art would not conceive a mechanism that monitors the read and write requests on a main storage unit and reduces the writing to the main storage unit to optimize network resources. Thus, reducing the writing to the storage mechanism is not obvious in view of Chiou.

Claim 1 as now presented includes, inter alia: a "storage system, comprising: . . . a storage mechanism access manager for monitoring read and write loading of the storage mechanism and for controlling the read and write directors and the cache manager in accordance with the storage mechanism read and write loading, wherein controlling the write directors includes reducing writing to the storage mechanism.

Claim as now presented includes, inter alia: a "method for storing content, comprising the steps of: . . . controlling reading of content from, and writing of content to the storage mechanism in accordance with the storage mechanism read and write loading, wherein controlling includes reducing writing to the storage mechanism."

Accordingly, claims 1 and 11 are novel over Chiou at least because Chiou does not disclose reducing writing to a main storage device in a cache system. Thus claims 1 and 11 are believed to be in condition for allowance. In addition, claims 2, 4-10, 12, 15 and 16 are believed to be in condition for allowance due at least to their dependencies from claims 1, 11.

It should be noted that applicants disagree with the examiner's assertion that claims 10 and 16 are anticipated by Chiou.

Claim 10 includes, inter alia: a system wherein a "storage mechanism access manager controls the read and write directors to reduce reading from, and writing to the storage mechanism during intervals of limited storage mechanism bandwidth." Similarly, claim 16

includes, inter alia: a method comprising "the step of restricting access to the storage mechanism during intervals of high bandwidth demand."

On pages 9 and 10-11, the examiner asserts that claims 10 and 16 are anticipated by Chiou and cites a section of Chiou's specification stating that the type of caching may be file based or block based. The entire cited section discusses the manner of storing cache data, not data stored in a main storage device. It is unclear how the cited section relates to reducing writing to or restricting access to a main storage device. In any event, the cited section of Chiou does not disclose reducing writing to or restricting access to a main storage device during periods of high bandwidth demand. Accordingly, claims 10 and 16 are not anticipated by Chiou.

Claims 3, 13 and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chiou in view of Tremblay, et al. (U.S. Patent Application Publicaiton No. 2002/0184460 A1) (hereinafter 'Tremblay').

It should first be noted that claims 3, 13 and 14 are believed to be in condition for allowance due at least to their dependencies on claims 1 and 11. However, there are other reasons for allowing the claims.

Claim 3 includes, inter alia: "a filler storage unit for storing filler content, and wherein [a] read director directs the read request to the filler storage unit to provide filler content when the requested content is unavailable from the local storage cache unit and insufficient bandwidth exists to access the storage mechanism."

Similarly, claim 13 includes, inter alia: "re-directing the content request to a filler storage unit to provide filler content if the requested content does not reside at the local cache storage unit and insufficient bandwidth exists to access the storage mechanism."

In the office action, the examiner states that claims 3 and 13 are unpatentable because Tremblay discloses the above quoted features of claims 3 and 13 and it would have been obvious to one of ordinary skill in the art to combine Chiou and Tremblay.

Tremblay discloses a method and apparatus for writing data into memory by combining data from a plurality of write transactions and writing data to memory in one write transaction (Tremblay, Abstract). Data is written into a storage device by employing memory store instructions. Tremblay states that in one embodiment of its system, "the format of the memory store instruction . . . includes: (1) a write command; (2) four beats of data (corresponding to a full cache line); (3) byte enable information specifying which or how many of the bytes in the four beats of data are to be actually written in memory; and (4) the address in main memory at which the specified bytes are to be written." (Tremblay, paragraph 23) (emphasis added).

Tremblay's method and system may be directed to "store pair instructions," which specify that one beat of data is to be written in main memory (Tremblay, paragraph 26). The store pair instruction includes: "(1) a write command to write data in main memory; (2) one beat of data to be written in main memory and three beats of unused or filler data; (3) byte enable information specifying which bytes of the one beat of data is to be actually written in memory; and (4) the address in main memory at which the specified bytes of the one beat are to be written." (Tremblay, paragraph 27) (emphasis added).

The three beats of filler data disclosed in Tremblay are used merely to follow the general format of having total four beats of data in a memory store instruction. The filler data is not used as a substitute for real data.

As stated above, according to one aspect of the present principles, filler content is provided in response to a read request for content if the cache does not contain the content and

there is insufficient bandwidth to access the storage mechanism. The filler content is used as a substitute for real data.

Accordingly, claims 3 and 13 are distinguished from Tremblay at least because Tremblay fails to disclose using filler content as a substitute for real content. Thus, claims 3 and 13 are believed to be in condition for allowance. Moreover, claim 14 is believed to be in condition for allowance due at least to its dependency from claim 13.

In view of the foregoing, the applicants respectfully request that the rejections of the claims set forth in the Office Action of March 28, 2007 be withdrawn, that pending claims 1-16 be allowed, and that the case proceed to early issuance of Letters Patent in due course.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicants' representatives Deposit Account No. 07-0832.

Respectfully submitted,

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